WHAT IS CLAIMED IS:

1. A single electron memory device comprising:

a substrate on which a nano-scale channel region is formed between a source and a drain; and

a gate lamination pattern including quantum dots on the channel region; and

wherein the gate lamination pattern includes:

a lower layer formed on the channel region;

a single electron storage medium formed on the lower layer, for storing a single electron tunneling through the lower layer;

an upper layer, including a plurality of quantum dots, formed on the single electron storage medium; and

a gate electrode formed on the upper layer to be in contact with the quantum dots.

2. The single electron memory device as claimed in claim 1, wherein the plurality of quantum dots are included in the upper layer and are isolated from the single electron storage medium.

3. The single electron memory device as claimed in claim 1, wherein the plurality of quantum dots are included in the upper layer and contact the single electron storage medium.

4. The single electron memory device as claimed in claim 1, wherein the upper layer is formed of a first and a second upper layer and the plurality of quantum dots are included in the second upper layer.

5. The single electron memory device as claimed in claim 1, wherein the single electron storage medium is formed of a material selected from the group consisting of silicon nitride (Si_3N_4), PZT, silicon (Si), silicon germanium (SiGe), gallium arsenide (GaAs), and a metal.

6. The single electron memory device as claimed in claim 2, wherein the single electron storage medium is formed of a material selected from the group consisting of silicon nitride (Si_3N_4), PZT, silicon (Si), silicon germanium (SiGe), gallium arsenide (GaAs), and a metal.

7. The single electron memory device as claimed in claim 3, wherein the single electron storage medium is formed of a material selected from the group consisting of silicon nitride (Si_3N_4), PZT, silicon (Si), silicon germanium (SiGe), gallium arsenide (GaAs), and a metal.

8. The single electron memory device as claimed in claim 1, wherein the lower layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

9. The single electron memory device as claimed in claim 1,

wherein the upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

10. The single electron memory device as claimed in claim 1, wherein the gate electrode is formed of a material selected from the group consisting of doped Si, doped SiGe, doped GaAs, a metal, a silicide, and a polycide.

11. The single electron memory device as claimed in claim 1, wherein the plurality of quantum dots are preferably formed of silicon.

12. A single electron memory device comprising:

a substrate on which a nano-scale channel region is formed between a source and a drain; and

a gate lamination pattern including quantum dots on the channel region; and

wherein the gate lamination pattern includes a lower layer, an upper layer, and a gate electrode, which are sequentially formed on the channel region, and a plurality of vertically spaced-apart first and second quantum dots included in the upper layer, the first quantum dots being in contact with the lower layer, and the second quantum dots being in contact with a bottom surface of the gate electrode.

13. A single electron memory device comprising:

a substrate on which a nano-scale channel region is formed between a source and a drain; and

a gate lamination pattern including a plurality of quantum dots on the channel region,

wherein the gate lamination pattern comprises:

a lower layer formed on the channel region;

a single electron storage means formed on the lower layer, for storing a single electron tunneling through the lower layer;

an upper layer covering the single electron storage medium, the upper surface of the upper layer being uneven; and

a gate electrode formed on the upper layer.

14. The single electron memory device as claimed in claim 13, wherein the single electron storage means is formed of a material selected from the group consisting of silicon nitride (Si_3N_4), silicon (Si), silicon germanium (SiGe), gallium arsenide (GaAs), and a metal.

15. The single electron memory device as claimed in claim 13, wherein the single electron storage means is a plurality of quantum dots formed on the lower layer.

16. The single electron memory device as claimed in claim 8, wherein the lower layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

17. The single electron memory device as claimed in claim 8, wherein the upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

18. The single electron memory device as claimed in claim 8, wherein the gate electrode is formed of a material selected from the group consisting of doped Si, doped SiGe, doped GaAs, a metal, a silicide, and a polycide.

19. The single electron memory device as claimed in claim 8, wherein the plurality of quantum dots are preferably formed of silicon.

20. The single electron memory device as claimed in claim 9, wherein the lower layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

21. The single electron memory device as claimed in claim 9, wherein the upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

22. The single electron memory device as claimed in claim 9, wherein the gate electrode is formed of a material selected from the group consisting of doped Si, doped SiGe, doped GaAs, a metal, a silicide, and a polycide.

23. The single electron memory device as claimed in claim 9, wherein the plurality of quantum dots are preferably formed of silicon.

24. A method for manufacturing a single electron memory device including a single electron storage element in a gate lamination pattern formed on a nano-scale channel region of a MOSFET, wherein formation of the gate lamination pattern comprises:

(a) sequentially forming a lower layer and a single electron storage medium for storing a single electron tunneling through the lower layer on a substrate;

(b) forming an upper layer including a plurality of quantum dots on the single electron storage medium;

(c) forming a gate electrode layer on the upper layer to be in contact with the plurality of quantum dots; and

(d) patterning the lower layer, the single electron storage medium, the upper layer, and the gate electrode layer, in reverse order.

25. The method as claimed in claim 24, wherein the formation of the upper layer comprises:

forming a first upper layer on the single electron storage medium;

forming the plurality of quantum dots on the first upper layer; and

forming a second upper layer to cover the plurality of quantum dots on the first upper layer.

26. The method as claimed in claim 24, wherein the formation of the gate electrode layer further comprises polishing the upper layer until the plurality of quantum dots are exposed before forming the gate electrode layer on the upper layer.

27. The method as claimed in claim 25, wherein the formation of the gate electrode layer further comprises polishing the second upper layer until the plurality of quantum dots are exposed before forming the gate electrode layer on the second upper layer.

28. The method as claimed in claim 24, wherein the formation of the upper layer further comprises:

forming the plurality of quantum dots on the single electron storage medium; and

forming the upper layer to cover the plurality of quantum dots on the single electron storage medium.

29. The method as claimed in claim 28, wherein the formation of the gate electrode layer further includes polishing the upper layer until the

plurality of quantum dots are exposed before forming the gate electrode layer on the upper layer.

30. The method as claimed in claim 24, wherein the single electron storage medium is formed of a material selected from the group consisting of silicon nitride (Si_3N_4), PZT, silicon (Si), silicon germanium (SiGe), gallium arsenide (GaAs), and a metal.

31. The method as claimed in claim 24, wherein the plurality of quantum dots contact the single electron storage medium and a bottom surface of the gate electrode.

32. The method as claimed in claim 24, wherein the plurality of quantum dots are formed by method selected from the group consisting of a selective growth method, a self-assembled growth method and a nano-scale lithography method.

33. A method for manufacturing a single electron memory device including a single electron storage element in a gate lamination pattern formed on a nano-scale channel region of a MOSFET, wherein the formation of the gate lamination pattern comprises:

(a) forming a lower layer on a substrate;

(b) forming an upper layer including a plurality of vertically spaced-apart first and second quantum dots on the lower layer;

(c) forming a gate electrode on the upper layer to be in contact with the plurality of second quantum dots; and

(d) patterning the lower layer, the upper layer, and the gate electrode, in reverse order.

34. The method as claimed in claim 33, wherein the formation of the upper layer comprises:

forming the plurality of first quantum dots on the lower layer, to store a single electron tunneling through the lower layer;

forming a first upper layer having a thickness sufficient to cover the plurality of first quantum dots;

forming the plurality of second quantum dots on the first upper layer; and

forming a second upper layer to cover the plurality of second quantum dots on the first upper layer.

35. The method as claimed in claim 34, wherein the formation of the gate electrode comprises polishing the second upper layer until the plurality of second quantum dots are exposed before forming the gate electrode on the second upper layer.

36. The method as claimed in claim 34, wherein the lower layer is formed of a material selected from the group consisting of silicon oxide

(SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

37. The method as claimed in claim 34, wherein the first upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

38. The method as claimed in claim 34, wherein the second upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), and titanium oxide (TiO_2).

39. The method as claimed in claim 34, wherein the gate electrode is formed of a material selected from the group consisting of doped Si, doped SiGe, doped GaAs, a metal, a silicide, and a polycide.

40. The method as claimed in claim 34, wherein the plurality of quantum dots are formed of silicon.

41. The method as claimed in claim 34, wherein the plurality of quantum dots are formed by a method selected from the group consisting of a selective growth method, a self-assembled growth method and a nano-scale lithography method.

42. A method for manufacturing a single electron memory device including a single electron storage element in a gate lamination pattern formed on a nano-scale channel region of a MOSFET, wherein the formation of the gate lamination pattern comprises:

(a) forming a lower layer on a substrate;

(b) sequentially forming a single electron storage means for storing a single electron tunneling through the lower layer, and an upper layer covering the single electron storage means, on the lower layer, wherein the surface of the upper layer is uneven;

(c) forming a gate electrode layer on the upper layer; and

(d) patterning the lower layer, the single electron storage means, the upper layer, and the gate electrode layer, in reverse order.

43. The method as claimed in claim 42, wherein the single electron storage means is a single electron storage medium and is formed of a material selected from the group consisting of silicon nitride (Si_3N_4), silicon (Si), PZT, silicon germanium (SiGe), gallium arsenide (GaAs), and a metal.

44. The method as claimed in claim 42, wherein the single electron storage means is a plurality of quantum dots.

45. The method as claimed in claim 42, wherein the lower layer is formed of a material selected from the group consisting of silicon oxide

(SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

46. The method as claimed in claim 42, wherein the upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

47. The method as claimed in claim 42, wherein the gate electrode is formed of a material selected from the group consisting of doped Si, doped SiGe, doped GaAs, a metal, a silicide, and a polycide.

48. The method as claimed in claim 42, wherein the plurality of quantum dots are formed of silicon.

49. The method as claimed in claim 42, wherein the lower layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

50. The method as claimed in claim 42, wherein the upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

51. The method as claimed in claim 42, wherein the gate electrode is formed of a material selected from the group consisting of doped Si, doped SiGe, doped GaAs, a metal, a silicide, and a polycide.

52. The method as claimed in claim 44, wherein the plurality of quantum dots are formed of silicon.

53. The method as claimed in claim 44, wherein the plurality of quantum dots are formed by a method selected from the group consisting of a selective growth method, a self-assembled growth method and a nano-scale lithography method.